

T.E (ELECTRONICS & TELECOMMUNICATION)

SEM .V

Computer Architecture & Organization

Lecture : 3p/week
Tutorial: 1p/week

Paper 100marks, 3 hrs
Term work: 25 marks

1. Introduction:

History and evolution of computers, architecture of general-purpose computer, stored program computer operation.

2.Data path design:

Computer system design, gate level design, register level design and processor level design, fixed point arithmetic, data paths of 2's complement addition subtraction, multiplication and division, Booth's algorithm for multiplication, floating point arithmetic and data path of floating point ALU.

3. Processor Design:

CPU organization and operation, accumulator based CPU, CPU with general registers, instruction types, formats and addressing arithmetic- logic unit design, sequential ALU's, structure of a basic sequential ALU, register files, co-processors and pipeline processors, RISC and CISC computers.

4. Control Design

General structure of hardwired and micro-programmed control units, hardwired control design, state tables, greatest common divisor processor, classical design of the gad processor control unit, design of a typical CPU control unit, micro- programmed control, control unit organization, microinstruction addressing and timing, micro-program sequencers, pipeline control, instruction pipeline, structure multistage pipeline, organization of CPU with multistage instruction pipeline, pipeline performance, measures.

5. Memory Organization:

Organization of multilevel memory system in a computer, main memory, random access memory organization, semiconductor RAM'S, RAM's design structure of a D-RAM chip, secondary memory, several access memory, access methods, memory organization magnetic disc and tape reluctant array of inexpensive disks, memories, optical memory and read-out devices.

6. High speed cache memory system:

Cache and virtual memory, address transformation with segmentation and paging with caches, cache organization, operation address mapping associate memory, cache types and performance.

7. System buses and I/O communication:

Buses, bus interfacing timing bus arbitration, I/O and system control, I/O control methods, programmed I/O, I/O instruction types, IOP organization, CPU and IOP interaction.

8. Multiple Advanced Processor organizations:

Parallel processing shared and distributed memory computers, processor interconnection network structures and performance, multiprocessors (MIMD).

Term Work:

Each student has to appear for at least one written Test during the term. All east eight assignments along with a graded

Answer paper shall be submitted as term work.

The distribution will be as follows:

Assignments - 15 marks:
Written Test - 10 marks.

Text books:

1. Computer architecture and organization- John P. Hayes.

Reference books:

1. Computer organization and architecture- William Stallings
Prentice Hall of India.
2. Computer organization- V Carl Hamacher and Zaky
Tata MC-Graw Hill publication.