

University Of Mumbai				
Class: S.E.	Branch: Computer Engineering	Semester:III		
Subject: Computer Organization and Architecture(Abbreviated as COA)				
Periods per week(each 60 min)	Lecture	03		
	Practical	02		
	Tutorial	--		
Evaluation System		Hours	Marks	
		Theory	03	100
		Practical and oral	--	--
		Oral	--	--
		Term work	--	25
	Total	03	125	

Module	Contents	Hours
1	Basic Structure of Computer Introduction of computer system and its sub modules, Basic organization of computer and block level description of the functional units. Von newmann model, Introduction to buses and connection I/O devices to CPU and memory, Asynchronous and Synchronous bus, PCI,SCSI	04
2	Arithmetic and logic Unit. Arithmetic and Logical unit hardware implementation, Booth's Recording, Booth's algorithm for signed multiplication, Restoring division and non restoring division algorithm,IEEE floating point number representation and operation.	07
3	Central Processing Unit CPU architecture, Register organization, Instruction formats and addressing modes(Intel processor).,Basic instruction cycle, Instruction interpretation and sequencing, Control unit, basic concepts. Microinstruction sequencing and execution, Micro operation, concepts of nanoprograming examples of RISC processors.	08
4	Memory Organization. Characteristics of memory system and hierarchy, concepts of semiconductor memories ,mainmemory ,ROM ,EPROM ,RAM ,SRAM ,DRAM ,SDRAM ,Flash memory ,stack organization, High speed memories: cache memory organization and mapping, replacement algorithms, cache coherence, Interleaved and associative memories, virtual memory, main memory allocation, segmentation paging, secondary storage ,RAID, optical memory ,CDROM,DVD	07

5	I/O Organization Input /Output Systems, Programmed I/O, Interrupt driven I/O, I/O channels, DMA, Peripheral Device , U.S.B.	03
6	Multiprocessor Configurations Flynn’s classification, Parallel processing concepts, Introduction to pipeline processing and pipeline hazards, design issues of pipeline architecture, Instruction pipeline, Instruction level parallelism and advanced issues.	04
7	SPARC Static and Dynamic data flow design, Fault tolerant computers, Interprocessor communication and synchronization, cache coherence, shared memory multiprocessor.	03
8	Systolic Architectures Systolic arrays and their applications, wave front arrays	02

TERM WORK

Based on above syllabus at least 10 experiments and one written test of 10 marks to be conducted.

Text Books:-

1. Miles Murdocca, “Computer Architecture and Organization “, Wiley India.
2. William Stallings, “Computer Organization and Architecture: Designing and performance”: Prentice-Hall India.
3. Carl Hamacher, Zvonko Vranesic and Safwat Zaky “Computer Organization”, McGraw Hill

Reference Books:-

1. John L. Hennessy and David Patterson,” Computer Architecture A Quantitative Approach”, Morgan Kaufman
2. Andrew S. Tanenbaum, “ Structured Computer Organization”, Prentice –Hall India.