

University of Mumbai				
Class: S.E.		Branch: Computer Engineering	Semester: III	
Subject: Digital Logic Design & Application (Abbreviated as DLDA)				
Periods per Week (each 60 min.)	Lecture		03	
	Practical		02	
	Tutorial		-	
		Hours	Marks	
Evaluation System	Theory		03	100
	Practical & Oral		-	-
	Oral		-	-
	Term Work		-	25
	Total		03	125

Module	Contents	Hours
1.	Number system :Decimal, Binary, Octal,& Hexadecimal number & conversion, Number system's application e.g. shaft encoding. Binary weighted codes , signed numbers binary order, 1's,2's compliments codes. All number system's arithmetic. Boolean algebra :Binary logic functions, Boolean laws, Truth Tables. Associative & distributive properties. Demorgan's Theorem. Realization of switching functions using logic gates.	07
2.	Combinational logic : Switching equations, Canonical logic forms, Sum of product & Product of sum , karnaugh Map, two, three & four variable karnaugh graph , Simplification of expression QuineMcCluskey minimization techniques, Mixed logic combinational Circuits, Multiple output functions.	06
3.	Analysis & design of combinational logic : Introduction of Combinational circuits. Multiplexer & demultiplexer, Multiplexer as function generator ,Binary adder, Subtractor ,BCD adder, Binary comparator with physical applications, Arithmetic & logic units, Design of combinational circuits using statements.	07

4.	Sequential Logic : Sequential circuits, Flip-Flop conversions, Clocked & edge triggered flip flops timing specification, Timing analysis, state diagrams & tables, transition tables, Excitation table & equation ,examples using statement.	05
5.	Sequential Circuits: Simple synchronous & asynchronous Sequential Circuits analysis, Different types of counters asynchronous & synchronous, Counter Design with state equations, Registers, Different types of Shift register, Construction of state diagram & counter design.	06
6.	Digital integrated circuits: Digital circuit logic levels, propagation delay times, power dissipation ,Fan out & Fan in. Noise margin for popular logic families. TTL ,TTI sub families. CMOS & their performance comparison (Numerical expected)	05

Term work

1. Term work should consist of at least 8 practical experiment duly graded(Desirable 10 experiment) & two assignments covering all the topics of the syllabus.
2. A term work test must be conducted with a weightage of 10 marks covering complete syllabus.

List of experiment:

1. Study of Basic Gates & universal gates.
2. Realization of logical expression using Universal Gates& Basic gates.
3. Binary Arithmetic circuits 1)Adder 2) Substracter.
4. Implement certain function using multiplexer [16:1 ,8:1 ,4:1]
5. Design & implement 4:1 multiplexer with strobe 1/p active low using NAND & NOR Gate.
6. To design & implement any one code converter [e.g. Excess-3,BCD—Gray]
Using Decoder & demultiplexer.
7. To design & implement 4-bit parity generator /checker using

- 1) Minimum number of gates .
 - 2) IC 74180.
8. Design of 7-segment display using decoder [IC 7447]
 9. Design of JK Flip flop using NAND Gates & verification of the same flip flop Using IC7476.
 10. Design of asynchronous up & Down counter.
 11. Design of synchronous Counter.
 12. Design of random sequence generator.
 13. Design of shift register using flip-flop verification of different modes.
 14. verification of function table of universal shift register IC 74194.
 15. Compare propagation delay & transfer characteristics of TTL & CMOS gates [use odd no. of gates]

Text Books:

1. R. P. Jain , "Modern Digital Electronics", Tata McGraw Hill.
2. John F. Warrly, "Digital Design Principles & Practices", Pearson Education ,Russia.
3. M ..Morris Mano, "Digital Logic & computer Design", PHI

Reference Books:

1. John M . yarbrough , "Digital Logic " Thomson Learning.
2. Samuel Lee , "Digital Circuits & Logic Design ", PHI.
3. Charles H. Roth, "Fundamentals of Logic Design, (4th edition), junior jaico Book.